Claim Amendments

Claim 1 (currently amended): A switch for switching packets from a plurality of sources comprising:

a port card having a striper;

a plurality of fabrics including a parity fabric, the striper sending different portions of the packet as stripes to each fabric and sends a parity stripe to perform error detection and correction to the parity fabric, each fabric having:

a memory in which portions of the packet are stored; and

a transferring mechanism which transfers predetermined portions of the packet to the memory as the predetermined portions are received, the transferring mechanism transfers predetermined portions of the packet as fixed length segments as the fixed length segments are received, followed by a single final segment of any length less than or equal to the length of the fixed length segments wherein the packet is transferred to the memory to smooth out bursts caused by lengthy packets.

Claim 2 (canceled)

Claim 3 (previously presented): A switch as described in Claim 1 wherein the transferring mechanism transfers fixed length segments of different packets interleaved among each other as they are received to the memory.

Claim 4 (original): A switch as described in Claim 3 wherein the transferring mechanism includes an aggregator which receives portions of packets from the plurality of sources.

Claim 5 (original): A switch as described in Claim 4 wherein the memory includes a memory controller.

Claim 6 (original): A switch as described in Claim 5 wherein the aggregator uses TDM to multiplex segments of packets from different sources to the memory controller.

Claim 7 (original): A switch as described in Claim 6 wherein the aggregator places an identifier with each segment identifying from which source the segments came from.

Claim 8 (original): A switch as described in Claim 7 wherein the memory controller includes per source queues, and stores each segment in a corresponding per source queue based on the identifier of the segment.

Claim 9 (previously presented): A switch as described in Claim 8 wherein the memory controller includes per destination queues, and once all segments for the packet are received at a per source queue, all the segments of the packet are changed to a corresponding per destination queue.

Claim 10 (original): A switch as described in Claim 9 wherein the memory controller has acceptance criteria for accepting segments, and if the segment is not accepted, then all previously received segments associated with the segment not accepted are purged from the per source queue and any segments associated with the segment not accepted that are received after the segment that was not accepted was received, are ignored.

Claim 11 (previously presented): A switch as described in Claim 10 including a separator disposed in the fabric connected to the aggregator.

Claim 12 (previously presented): A switch as described in Claim 11 wherein the port card includes an unstriper which receives portions of packets from the separator.

Claim 13 (original): A switch as described in Claim 12 wherein the memory controller includes a shared memory, and the destination queues and the source queues are part of the shared memory.

Claim 14 (currently amended): A method for switching packets comprising the steps of:

sending from a port card different portions of a packet as stripes to each of a plurality of fabrics of a switch and a parity stripe which performs error detection and correction to a parity fabric;

receiving portions of the packet at a transferring mechanism of each fabric; and

transferring predetermined portions of the packet to a memory of each fabric as fixed length segments as the fixed length segments are received at the transferring mechanism followed by a single final segment of any length less than or equal to the length of the fixed length segments wherein the packet is transferred to the memory to smooth out bursts caused by lengthy packets.

Claim 15 (canceled)

Claim 16 (previously presented): A method as described in Claim 14 wherein the transferring step includes the step of transferring fixed length segments of different packets as they are received interleaved among each other to the memory.

Claim 17 (previously presented): A method as described in Claim 16 wherein the receiving step includes the step of receiving portions of packets from different sources at an aggregator of the transferring mechanism disposed in each fabric of the switch.

Claim 18 (previously presented): A method as described in Claim 17 wherein the transferring step includes the step of multiplexing with the aggregator segments of packets from different sources to a memory controller.

Claim 19 (original): A method as described in Claim 18 wherein before the transferring step, there is the step of placing by the aggregator an identifier with each segment identifying from which source the segment came from.

Claim 20 (original): A method as described in Claim 19 wherein after the transferring step, there is the step of storing each segment in a corresponding per source queue of the memory controller based on the identifier of the segment.

Claim 21 (original): A method as described in Claim 20 including after the storing step, there is the step of changing all segments of the packet in the source queue to a corresponding per destination queue of the memory controller once all the segments of the packet are received at the per source queue.

Claim 22 (original): A method as described in Claim 21 wherein the receiving step includes the steps of purging all previously received segments associated with an unaccepted segment that does not meet acceptance criteria for accepting a segment of the memory controller, and ignoring all segments associated with the unaccepted segment received at the memory controller after the unaccepted segment is received at the memory controller.

Claim 23 (previously presented): A method as described in Claim 22 wherein the receiving step includes the step of receiving portions of packets as stripes from different sources at the aggregator of the transferring mechanism disposed in each fabric of the switch from a striper of the port card of the switch.

Claim 24 (previously presented): A method as described in Claim 23 including after the moving step, there is the step of sending portions of the packet from the memory controller with a separator of each fabric to an unstriper of the port card.

Claim 25 (previously presented): A switch for switching packets from a plurality of sources comprising:

a port card having a striper;

a plurality of fabrics, the striper sending portions of the packet as stripes to each fabric, each fabric having:

a memory in which portions of the packet are stored, the memory including memory controller, the memory controller has acceptance criteria for accepting segments, and if the segment is not accepted, then all previously received segments associated with the segment not accepted are purged from the per source queue and any segments associated with the segment not accepted that are received after the segment that was not accepted was received, are ignored; and

a transferring mechanism which transfers predetermined portions of the packet to the memory as the predetermined portions are received, the transferring mechanism transfers predetermined portions of the packet as fixed length segments as the fixed length segments are received, followed by a single final segment of any length less than or equal to

the length of the fixed length segments wherein the packet is transferred to the memory to smooth out bursts caused by lengthy packets.

Claim 26 (previously presented): A method for switching packets comprising the steps of:

sending from a port card portions of a packet as stripes to each of a plurality of fabrics of a switch;

receiving portions of the packet at a transferring mechanism of each fabric, the receiving step includes the steps of purging all previously received segments associated with an unaccepted segment that does not meet acceptance criteria for accepting a segment of the memory controller, and ignoring all segments associated with the unaccepted segment received at the memory controller after the unaccepted segment is received at the memory controller; and

transferring predetermined portions of the packet to a memory of each fabric as fixed length segments as the fixed length segments are received at the transferring mechanism followed by a single final segment of any length less than or equal to the length of the fixed

length segments wherein the packet is transferred to the memory to smooth out bursts caused by lengthy packets.